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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,426	03/31/2004	Phillip M. Matthews	81339624US01 (5797-00500)	5709

65913 7590 07/25/2007

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EXAMINER	
DALEY, CHRISTOPHER ANTHONY	
ART UNIT	**PAPER NUMBER**
2111	

NOTIFICATION DATE	DELIVERY MODE
07/25/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/814,426	MATTHEWS ET AL.	
	Examiner	Art Unit	
	Christopher A. Daley	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 – 56 are pending.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 –56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shaeffer et al (US6963626) hereinafter Shaeffer in view of Hadwiger et al (US6738845) hereinafter Hadwiger.

3. As to claims 1,21,26, 38, 42, 49, and 53 Shaeffer discloses a communication apparatus, method, and phone comprising: a radio frequency (RF) circuit for operating on a radio frequency signal; and a digital processing circuit coupled to the RF circuit, wherein the digital processing circuit includes:

a first bus master coupled to a bus (Figure 1 illustrates a processor comprising a bus master 12 coupled to a bus that couples memory 118 with processor 116, COL. 5, lines 46 - 63);

wherein accesses by the one or more other bus masters to the bus are restricted in response to a signal indicative of a change in a mode of operation of the RF circuit

(Time controller 110 is access controller to prevent noise coupling between the analog and digital circuitry, COL. 6, lines 1 - 10);

wherein accesses by the one or more other bus masters to the bus are restricted during a second period of operation in response to a signal asserted a predetermined amount of time prior to a shutdown mode of operation of the digital processing circuit (Time controller 110 comprises a programmed timer that restricts access by shutting down the clocking system via a delay locked loop, COL. 6, lines 10 - 17) .

Shaeffer does not explicitly disclose one or more other bus masters coupled to the bus; and configured to arbitrate between requests to access the bus by the first bus master and the one or more other bus masters;

wherein the bus arbiter is further configured to implement a less favorable arbitration policy for the one or more other bus masters in response to a signal indicating a change to an active mode of operation of the RF circuit.

However, Hadwiger teaches one or more other bus masters coupled to the bus; and a bus arbiter configured to arbitrate between requests to access the bus by the first bus master and the one or more other bus masters as system illustrated in figure 2 comprises multiples bus masters such as 201 and 202 with arbiter 211 that configures the common bus access between said masters, (COL. 4, lines 32 - 54).

This provides a cost effective solution for mobile phones that requires multiple processors, COL. 1, lines 25 - 40.

The arbitration module is programmed to afford less favorable access to devices not on the common local bus, (COL. 5, lines 10 - 22).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the processor of Shaeffer with the multiple processor core of Hadwiger to provide a cost effective solution for mobile phones that requires multiple processors, COL. 1, lines 25 - 40.

4. As to claims 2,23, and 27, are Shaeffer discloses the communication apparatus wherein the signal is indicative of a change to an active mode of operation of the RF circuit (Figure 7A illustrates the mode change from analog to digital, COL. 9, lines 27 - 39).

5. As to claim 3, Shaeffer discloses the communication apparatus wherein the signal indicates a change to a transmission mode of operation of the RF circuit (Figure 3 illustrates transmission mode from analog front end to digital circuitry, COL. 8, lines 1 - 10).

6. As to claim 4, Shaeffer discloses the communication apparatus as recited in claim 2 wherein the signal indicates a change to a reception mode of operation of the RF circuit (Figure 4 illustrates reception mode from digital circuitry to analog, COL. 8, lines 12 - 23).

7. As to claims 5, 28, 24, 34, and 43 Shaeffer discloses the communication apparatus wherein the signal is asserted a predetermined amount of time prior to the

change to the active mode of operation of the RF circuit (Said limitation illustrated in Figure 7C, COL. 9, lines 40 - 50).

8. As to claims 6,29,35,40,51 Shaeffer discloses the communication apparatus wherein the signal is asserted a predetermined amount of time prior to a shutdown mode of operation of the digital processing circuit (Said limitation is illustrated in Figure 7D, COL. 9, lines 45 - 50).

9. As to claims 7,30, 36, and 55, Shaeffer discloses the communication apparatus wherein the signal indicative of a change of mode of operation of the RF circuit is generated by a timing circuit (Figure 1 illustrates said timing circuit, timing controller 110, Col. 5, lines 46 - 63).

10. As to claims 8,25,31,37, 39, and 44 Hadwiger discloses the communication apparatus wherein the first bus master is provided exclusive access to the bus in response to assertion of the signal (When the first bus master assets control, it has exclusive access, page 4, paragraph 0044).

11. As to claims 9, and 45 Hadwiger discloses the communication apparatus wherein the first bus master is a microcontroller unit (MCU) (said limitation is depicted in figure 2, page 2, paragraph 0023).

12. As to claim 10, Hadwiger discloses the communication apparatus wherein the first bus master is a digital signal processor (DSP) (said limitation is depicted in figure 2, page 2, paragraph 0023).

13. As to claim 11, Hadwiger discloses The communication apparatus wherein an interrupt signal is provided to the MCU and wherein an interrupt service routine executed by the MCU in response to assertion of the interrupt signal is performed when accesses by masters other than the first bus master to the bus are restricted (Said limitation, page 4, paragraph 0044).

14. As to claim 12, Hadwiger discloses the communication apparatus wherein the interrupt service routine performs functionality to prepare the digital processing circuit for a shutdown mode of the digital processing circuit (Said limitation, page 4, paragraph 0044).

15. As to claim 13, Hadwiger discloses the communication apparatus wherein the bus is a multi-layer bus, wherein the first bus master is provided exclusive access to one layer of the bus in response to assertion of the signal while the one or more other bus masters are allowed access to another layer of the multi-layer bus (Multiple arbitration systems and buses are present to afford access to other bus system concurrently, page 2, paragraph 0023).

16. As to claims 14, and 51, Shaeffer discloses the communication apparatus wherein the shutdown mode of operation includes disabling at least a portion of the digital processing circuit (Figure 1 illustrates time controller disabling digital circuit 116, COL. 6, lines 5 - 10).

17. As to claim 15, 41, and 52, Shaeffer discloses the communication apparatus wherein the shutdown mode of operation includes disabling a clock that clocks at least a portion of the digital processing circuit (PLL or DLL controls clock, COL. 6, lines 10 - 17).

18. As to claim 16, Hadwiger discloses the communication apparatus wherein the bus arbiter is configured to restrict the granting of ownership of the bus to the one or more other bus masters in response to the signal (The arbiter module BAM of figure 2 dictates bus ownership, page 1, paragraph 0010).

19. As to claim 17, Hadwiger discloses the communication apparatus wherein the one or more other bus masters are configured to inhibit requests to gain ownership of the bus in response to the signal (The arbiter module BAM of figure 2 dictates bus ownership, page 1, paragraph 0010).

20. As to claim 18,22, 46, and 56 Hadwiger discloses the communication apparatus wherein accesses by the one or more other bus masters are restricted by implementing

a less favorable arbitration policy for the one or more other bus masters in response to the signal (The arbitration module is programmed to afford less favorable access to devices not on the common local bus, page 3, paragraph 0025).

21. As to claim 19, Hadwiger discloses the communication apparatus wherein accesses by the one or more other bus masters to the bus are restricted by terminating burst transfers early in response to the signal (The arbitration module is programmed to afford less favorable access to devices not on the common local bus, page 3, paragraph 0025).

22. As to claim 20, Shaeffer discloses the communication apparatus wherein the signal indicative of a change of mode of operation of the RF circuit is generated in response to execution of a software instruction (Figure 6 illustrates mode selection under software control, COL. 9, lines 7 - 15).

23. As to claim 22, Hadwiger discloses the method wherein accesses by the one or more bus masters are restricted by implementing a less favorable arbitration policy for the one or more bus masters in response to the signal (The arbitration module is programmed to afford less favorable access to devices not on the common local bus, page 3, paragraph 0025).

24. As to claim 47, Shaeffer discloses the communication apparatus wherein the interrupt service routine performs functionality to prepare the digital processing circuit for a shutdown mode of the digital processing circuit (Figure 6 illustrates control circuitry to perform said function, Col. 9, lines 7 - 15).

25. As to claims 50, and 54, Hadwiger discloses the mobile phone and communication apparatus wherein the first bus master is provided exclusive access to the bus during the second period of operation (Granting bus access by various modules, COL. 3, lines 23 - 40).

26. As to claim 32, Shaeffer/Hadwiger discloses a mobile phone comprising: a radio frequency (RF) front-end circuit for operating on a radio frequency signal;

Shaeffer teaches a digital processing circuit coupled to the RF front-end circuit, wherein the digital processing circuit includes a first bus master coupled to a bus and one or more other bus masters coupled to the bus (Figure 1 illustrates RF circuit 114 coupled to bus master 116); and

Hadwiger teaches a bus arbiter configured to arbitrate between requests to access the bus by the first bus master and the one or more other bus masters (first bus master and the one or more other bus masters as system illustrated in figure 2 comprises multiples bus masters such as 201 and 202 with arbiter 211 that configures the common bus access between said masters, (page 1, paragraph 0010);

Shaeffer teaches wherein accesses by the one or more other bus masters to the bus

are restricted in response to a signal indicative of a change in a mode of operation of the RF front-end circuit (Time controller 110 is access controller to prevent noise coupling between the analog and digital circuitry, COL. 6, lines 1 - 10); and wherein the RF front-end circuit and the digital processing circuit are fabricated on a single integrated circuit chip (Single chip embodiment, COL. 11, lines 23 – 27).

27. As to claim 33, Shaeffer discloses the mobile phone wherein the signal is indicative of a change to an active mode of operation of the RF front-end circuit (Figure 1 illustrates an interrupt signal 18 used to indicate the active mode of the RF circuit, Col. 2, lines 9 – 18).

28. As to claim 48, Shaeffer discloses the communication apparatus as recited in claim 42 wherein the RF circuit and the digital processing circuit are integrated on a single chip (SOC solution that integrates RF circuits, and digital circuits on the same piece of silicon, COL. 11, lines 23 – 27).

Response to Arguments

29. Applicant's arguments with respect to claims 1,21,26,38,42,49, and 53 have been considered but are moot in view of the new ground(s) of rejection. With regards to the applicant's argument that prior art does not teach restricting bus access in response to change in mode. Shaeffer teaches of an analog digital communication system comprising of an analog front end and processors coupled by a timing controller. Said

timing controller restricts bus access to prevent coupling of noise for the digital into analog circuitry. It provides a time-interleaved process for mode selection between the analog and digital portions of the system. Time controller 110 comprises a programmed timer that restricts access by shutting down the clocking system via a delay locked loop, COL. 6, lines 10 – 17. Therefore, the examiner cannot allow the claims, since the prior art discloses the element.

Conclusion

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher A. Daley whose telephone number is 571 272 3625. The examiner can normally be reached on 9 am. - 4p m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571 272 3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CAD
7/16/07

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